

# Design and cryogenic operation of a hybrid quantum-CMOS circuit

P. Clapera, S. Ray, X. Jehl, and M. Sanquer

*Univ. Grenoble Alpes, INAC-SPSMS, F-38000 Grenoble, France and  
CEA, INAC-SPSMS, F-38054 Grenoble, France*

A. Valentian and S. Barraud

*Univ. Grenoble Alpes, LETI-DCOS, F-38000 Grenoble, France and  
CEA, LETI, Minatec campus, F-38054 Grenoble, France*

Silicon-On-Insulator nanowire transistors of very small dimensions exhibit quantum effects like Coulomb blockade or single-dopant transport at low temperature. The same process also yields excellent field-effect transistors (FETs) for larger dimensions, allowing to design integrated circuits. Using the same process, we have co-integrated a FET-based ring oscillator circuit operating at cryogenic temperature which generates a radio-frequency (RF) signal on the gate of a nanoscale device showing Coulomb oscillations. We observe rectification of the RF signal, in good agreement with modeling.

While silicon-based complementary metal-oxide-semiconductor (CMOS) technology constitutes the mainstream of electronics, research for the beyond CMOS era focuses mostly on devices relying on new materials and/or quantum features<sup>1–3</sup>. Although circuits can be made with these advanced devices, like graphene-based oscillators<sup>4</sup> or single-electron transistors (SETs)<sup>5–7</sup>, a first step is to interface these quantum nanoelectronic devices with conventional CMOS circuits. The integration with mainstream technology is greatly simplified when the novel device is silicon-based. Hybrid circuits using a small number of field effect transistors (FETs) and SETs have been demonstrated<sup>8–13</sup>. Recently an SET device has been integrated with CMOS 1-bit selectors<sup>14</sup>. In this work SETs working up to 300K were obtained by very small nanowire cross sections resulting in shape fluctuations. Here we demonstrate the integration of an SET relying on well controlled dimensions<sup>15</sup> and a ring oscillator (RO) CMOS circuit designed for low temperature operation, made with more than 600 FETs. The different FET or SET behaviour is obtained by varying the width of transistors all fabricated with the fully-depleted silicon-on-insulator (FD-SOI) nanowire technology<sup>16</sup>. The RO output feeds a non-overlapping clock generators which delivers two, phase shifted square wave signals at radio frequency onto the gates of the SET device. When the RF is turned on we observe a dc current in the SET at zero source-drain bias, due to rectification effect. This effect naturally arises when sufficiently large RF signals are applied to a non-linear device<sup>17,18</sup>.

A schematic diagram of the whole circuit patterned on a 11 nm thick SOI film with the trigate SOI technology<sup>16</sup> is shown in Fig. 1. The SET is made with a 25 nm wide nanowire covered by 2 gates of length 40 nm. Only one of the two gates is used in this study. The gate stack consists of  $\approx 0.8$  nm of  $\text{SiO}_2$ ,  $\approx 2$  nm  $\text{HfSiON}$ , 5 nm of  $\text{TiN}$  and 50 nm of polycrystalline silicon. After gate etching a single, self-aligned 12 nm  $\text{Si}_3\text{N}_4$  spacer is deposited. The back-end process follows with

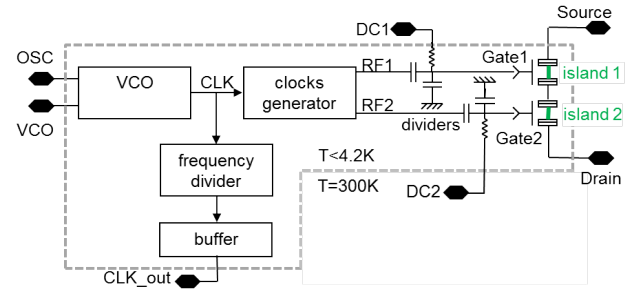


FIG. 1: Schematics of the whole circuit designed and fabricated on 300 nm SOI wafers. The nanowire dominated by Coulomb blockade below 10 K is on the right. The CMOS circuit driving the gates is made of several sub-circuits. A voltage controlled oscillator (VCO), monitored through a frequency divider, feeds a clock generator also based on ring-oscillators. This generator delivers two delayed and phase-shifted RF signals,  $RF1$  and  $RF2$ , which are further attenuated by capacitive dividers and added to external DC biases. The voltage supply  $V_{DD}$  referenced to ground  $GND$  is not shown.

epitaxy for raised source/drain, doping and silicidation (NiPtSi). The circuit for generating RF signals is made with  $2 \times 1 \mu\text{m}$  wide channels and 60 nm long gates. All the transistors are supplied with a voltage  $V_{DD}$  referenced to ground ( $GND$ ). The circuit starts with a Voltage-Controlled Oscillator (VCO) made of 20 inverters and 1 NAND gate. A voltage controlled current source is inserted in the inverters with an N-type FET in footer configuration. The VCO can be switched ON or OFF with the  $OSC$  input and its frequency is tuned by an external control voltage  $VCO$ . In agreement with simulations the VCO output frequency ranges from 300 kHz ( $VCO=0.2$  V) to 1.8 GHz ( $VCO=1$  V) at 300 K. It feeds a second, non-overlapping clock generator with two outputs. It is made of 5 buffers allowing to shift by 108 ps the two signals, ensuring that only one of the two outputs is in the high ( $V_{DD}$ ) state at any time. In addition the fre-

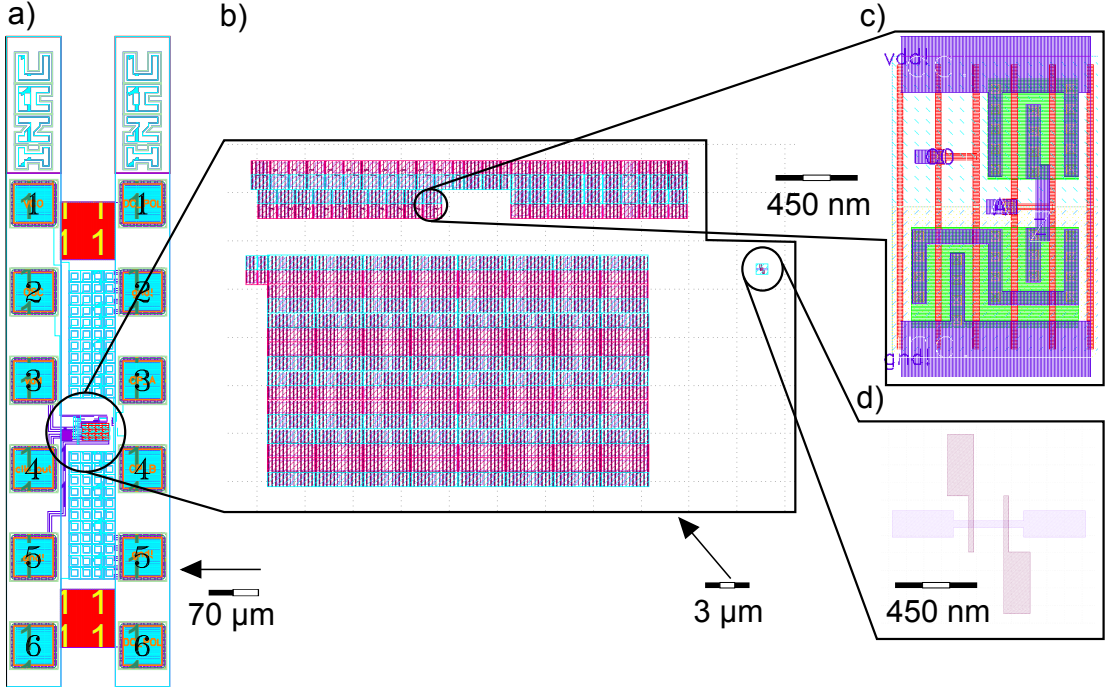


FIG. 2: **a)** View of the complete circuit layout with 12 contact pads, the bias resistors in red and capacitors as empty cyan squares between pads 2-3 and 4-5. **b)** Detailed view of the CMOS circuits located between pads 3 and 4. The top part is the VCO ( $\approx 130$  FETs) and non-overlapping clock generator ( $\approx 100$  FETs), while the bottom part is the frequency divider ( $\approx 400$  FETs). Both are made with  $1\mu\text{m}$  wide channels and  $60\text{ nm}$  long gates as depicted in **c)**. **c)** FET design with the gate level in red, the source and drain in purple and active area in green. **d)** Detailed view of the SET device ( $25\text{ nm}$  wide channel and  $40\text{ nm}$  long gates).

quency of the VCO is monitored by a frequency divider. The two outputs  $RF1$  and  $RF2$  are attenuated by capacitive dividers in order to lower their amplitudes down to  $0.5\text{ mV}$ , and they are added to two DC voltages  $DC1$  and  $DC2$  thanks to bias tees realized with  $1\text{ M}\Omega$  poly-silicon resistors. In the end  $DC1 + RF1$  and  $DC2 + RF2$  are respectively applied to gates 1 and 2 of the SET device.

The circuit implementation is shown in Fig. 2, with detailed views of the RO and SET. It uses 12 aluminium pads for external control (see Fig. 2a). The passive components of the circuits are the resistors (red squares) and the  $2\text{ pF}$  and  $1\text{ fF}$  capacitors (empty cyan squares in Fig. 2a) made between the two metal layers of the back-end process. The RO and frequency divider are located between pads 3 and 4 (see Fig. 2a and 2b).

The frequency response of the VCO is shown in Fig. 3 for various temperatures. The RO being fed by the output current of the N-FETs controlled by  $VCO$ , we obtain a curve similar to the drain-source vs. gate voltage characteristics of an N-FET, with a sub-threshold regime getting steeper as the temperature decreases and a saturation at  $1.36\text{ GHz}$  at  $300\text{ K}$  and  $1.06\text{ GHz}$  at  $4.2\text{ K}$ . This very good behaviour down to  $4.2\text{ K}$  of a CMOS circuit containing 600 approximately transistors shows that conventional silicon electronics is perfectly suitable for use at low temperature, provided that passive components such

as capacitors and mostly resistors are carefully designed.

Because of its small cross-section the quantum device driven by the CMOS circuit exhibits Coulomb blockade oscillations below  $\approx 10\text{ K}$ <sup>15,19</sup>, as shown in Fig. 4a where the low-frequency transconductance  $G_{diff}$  versus the gate voltage which is varied ( $V_g$ ) is shown at  $1\text{ K}$ . Four quasi-periodic peaks are observed, corresponding to the addition of 4 electrons in the channel below the gate. The period of  $18\text{ mV}$  in  $V_g$  corresponds to an effective gate capacitance of  $9\text{ aF}$ . These results are obtained without DC drain-source bias and no RF applied, hence there is no DC current flowing through the device in that case.

When the CMOS circuit is turned on, but still no DC bias applied, we measure a DC current, shown in Fig 4b. The presence of current in absence of bias and its characteristic dependence with  $V_g$  is well explained by a rectification effect. In nanoscale devices which are by principle difficult to contact perfectly, AC signals driven onto gates can induce a parasitic oscillatory source-drain bias<sup>17</sup>. For electron pumping experiments it is important to discriminate between this spurious current and the true pumped current<sup>17,18</sup>. Following these previous studies, we consider an RF driven gate voltage  $V_g(t) = V_g^{DC} + A\sin(2\pi ft)$  which couples capacitively to the source and drain, hence creating an additional AC bias component at the same frequency  $f$  in addition to

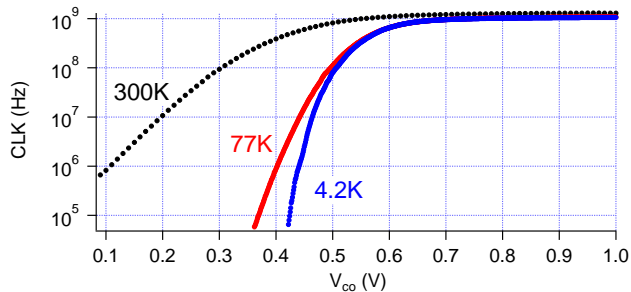


FIG. 3: Output frequency of the voltage-controlled oscillator measured at 300, 77 and 4.2 K after correction by the frequency divider (division by a factor of 65536). The maximum output frequency are 1.36 GHz at 300 K, 1.08 GHz at 77 K and 1.06 GHz at 4.2 K.

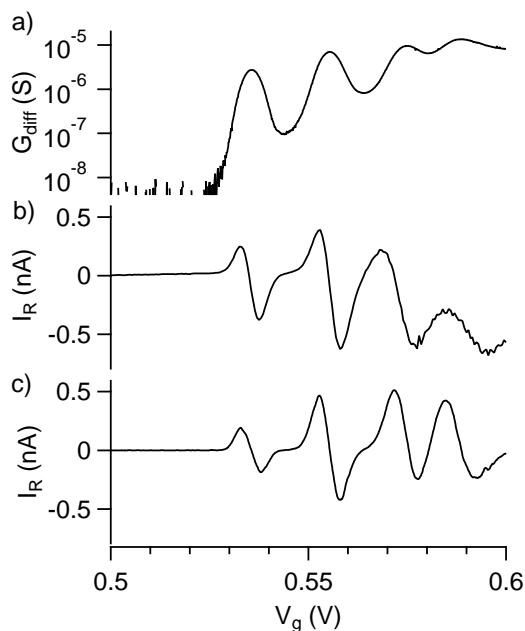


FIG. 4: **a)** Coulomb blockade oscillations measured at 1 K with a lock-in amplifier with an AC signal of  $100 \mu\text{V}$  at 77 Hz. **b)** DC current measured when  $V_{ds}^{DC}=0$  but CMOS circuit switched on, with amplitude  $500 \mu\text{V}$  at 412 MHz. **c)** DC current calculated with the rectification model. We find good agreement with the measured current shown in **b)**. The current follows the derivative of the transconductance, i.e. the second derivative of the conductance.

the DC bias  $V_{ds}^{DC}$ :

$$V_{ds}(t) = V_{ds}^{DC} + kV_{ds}^{AC} \sin(2\pi ft + \phi), \quad (1)$$

where  $k$  and  $\phi$  characterize the coupling. The rectified current is the average over one period  $\frac{1}{f}$  of the resulting current  $I(t) = V_{ds}(t)G(t)$ :

$$I_R = f \int_0^{1/f} V_{ds}(t)G(t)dt \quad (2)$$

As already pointed out in<sup>17</sup> and<sup>18</sup>, the general expression obtained by combining 1 and 2 is greatly simplified in the limit of small driving amplitude  $A$ . This is the standard case for AC lock-in measurements where one can use a linear approximation:  $I(t) \propto \frac{\partial G}{\partial V_g} |_{V_g=V_g^{DC}}$ . Here we are interested in the integral over one period (equation 2) to get the DC component, hence the same approximation is used again and

$$I_R \propto \frac{\partial^2 G}{\partial V_g^2} |_{V_g=V_g^{DC}}. \quad (3)$$

This model is used to calculate the rectified current  $I_R$  in the general case and taking into account our non-sinusoidal RF excitation by using the Fourier series describing a square wave instead of a single sine wave. The results are shown in Fig 4c. We found an excellent agreement with the measurements (Fig 4b) and recover the result that  $I_R$  is proportional to the second derivative of the conductance (equation 3). This is expected since we operate the circuit with RF output amplitude  $500 \mu\text{V}$ , which is small compared to the Coulomb oscillations period in the transconductance. Indeed this amplitude is of the order of the linewidth of the graph in Fig 4a.

## I. CONCLUSION

We have designed, fabricated and operated down to 4.2 K a circuit allowing to generate on-chip RF signals on the gates of a nanoscale quantum device. The clock generators based on a ring oscillator as well as the capacitance divider and bias resistors are fully operational down to 1 K. We have observed a finite DC current through the quantum device in the absence of DC bias when the RF drive is turned on. This current which scales with the derivative of the differential conductance is well understood within the framework of rectification due to capacitive coupling of the gate signal to the source and drain of the nanodevice. These results pave the way for the integration of conventional CMOS circuits operating at low temperatures together with quantum devices.

P. Clapera acknowledges support from the PhD program of the Nanosciences foundation in Grenoble. This work was partially supported by the EU through the FP7 ICT projects TOLOP (318397) and SiAM (610637), and by the Joint Research Project Qu-Ampere (SIB07) from the European Metrology Research Programme (EMRP). The EMRP is jointly funded by the EMRP participating countries within EURAMET and the European Union.

- 
- <sup>1</sup> *International technology roadmap for semiconductors, Emerging Research Devices* (2013)
  - <sup>2</sup> P. M. Koenraad and M. E. Flatte, *Nat Mater* **10**, 91 (2011)
  - <sup>3</sup> K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, *Nature* **490**, 192 (2012)
  - <sup>4</sup> D. Schall, M. Otto, D. Neumaier, and H. Kurz, *Sci. Rep.* **3**, 2592 (2013)
  - <sup>5</sup> Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K. Murase, *Appl. Phys. Lett* **76**, 3121 (2000)
  - <sup>6</sup> V. I. Conrad, A. D. Greentree, and L. C. L. Hollenberg, *Applied Physics Letters* **90**, (2007)
  - <sup>7</sup> C. K. Lee, S. J. Kim, S. J. Shin, J. B. Choi, and Y. Takahashi, *Applied Physics Letters* **92**, (2008)
  - <sup>8</sup> H. Inokawa, A. Fujiwara, and Y. Takahashi, *Electron Devices, IEEE Transactions on* **50**, 462 (2003)
  - <sup>9</sup> M. Saitoh, H. Harata, and T. Hiramoto, in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International* (2004) pp. 187–190
  - <sup>10</sup> S. Mahapatra and A. M. Ionescu, *Hybrid CMOS Single-Electron-Transistor Device and Circuit Design* (Artech House, 2006)
  - <sup>11</sup> K. Nishiguchi, A. Fujiwara, Y. Ono, H. Inokawa, and Y. Takahashi, *Applied Physics Letters* **88**, 183101 (2006)
  - <sup>12</sup> W. Zhang, N.-J. Wu, T. Hashizume, and S. Kasai, *Nanotechnology, IEEE Transactions on* **6**, 146 (2007)
  - <sup>13</sup> V. Deshpande, R. Wacquez, M. Vinet, X. Jehl, S. Barraud, R. Coquand, B. Roche, B. Voisin, C. Vizioz, B. Previtali, L. Tosti, P. Perreau, T. Poiroux, M. Sanquer, B. De Salvo, and O. Faynot, in *Electron Devices Meeting (IEDM), 2012 IEEE International* (2012) pp. 8.7.1–8.7.4
  - <sup>14</sup> R. Suzuki, M. Nozue, T. Saraya, and T. Hiramoto, *Japanese Journal of Applied Physics* **52**, 04CJ05 (2013)
  - <sup>15</sup> M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, and S. Deleonibus, *Applied Physics Letters* **89**, 143504 (2006)
  - <sup>16</sup> S. Barraud, R. Coquand, M. Casse, M. Koyama, J. Hartmann, V. Maffini-Alvaro, C. Comboroure, C. Vizioz, F. Aussenac, O. Faynot, and T. Poiroux, *Electron Device Letters, IEEE* **33**, 1526 (Nov 2012)
  - <sup>17</sup> P. W. Brouwer, *Phys. Rev. B* **63**, 121303 (Mar 2001)
  - <sup>18</sup> S. P. Giblin, M. Kataoka, J. D. Fletcher, P. See, T. J. B. M. Janssen, J. P. Griffiths, G. A. C. Jones, I. Farrer, and D. A. Ritchie, *Journal of Applied Physics* **114**, (2013)
  - <sup>19</sup> V. Deshpande, S. Barraud, X. Jehl, R. Wacquez, M. Vinet, R. Coquand, B. Roche, B. Voisin, F. Triozon, C. Vizioz, L. Tosti, B. Previtali, P. Perreau, T. Poiroux, M. Sanquer, and O. Faynot, *Solid-State Electronics* **84**, 179 (2013)